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Fig. 7 illustrates a third embodiment, appropriate for use in conjunction with two-stage input receivers. This embodiment comprises a plurality of two-stage input receivers 302, and a reference receiver or buffer 304. Input inductance and capacitance are represented in Fig. 7 as L_I and C_I , respectively. The circuit receives a plurality of signal voltages V_{SIGEXT} , which are subject to input inductance L_I and capacitance C_I to produce internal signal voltages referred to as V_{SIG} . The circuit also receives a voltage reference signal V_{REF} , which is similarly subject to input inductance L_I and capacitance C_I to produce internal reference voltages referred to as V_{REFU} and V_{REFD} .

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Reference receiver 304 receives the distributed voltage V_{REFD} , and an undistributed voltage V_{REFU} . V_{REFU} is a voltage or signal that has not been distributed to all of the signal receivers. In this embodiment, the undistributed reference voltage is connected [[to]] only to the single reference receiver 304.